Claims

1. A semiconductor device, comprising:

a substrate including a dopant of a first polarity;

a first semiconducting structure including a dopant of a second polarity and disposed over said substrate, said first semiconducting structure having substantially planar top and side surfaces;

a first junction formed between said first semiconducting structure and said substrate, said first junction having an area having at least one lateral dimension less than about 75 nanometers.

2. The semiconductor device in accordance with claim 1, further comprising:

a second semiconducting structure including a dopant of said first polarity formed on said first semiconducting structure said second semiconducting structure having substantially planar top and side surfaces; and

a second junction formed between said first semiconducting structure and said second semiconducting structure, said second junction having a length and a width, and said second junction having an area having at least one lateral dimension less than about 75 nanometers.

3. The semiconductor device in accordance with claim 1, wherein said first semiconducting structure further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting structure further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting lines.

4. The semiconductor device in accordance with claim 3, wherein said epitaxial semiconducting lines and said first semiconducting lines form an array of bipolar junction transistors having at least one junction having a junction area having at least one lateral dimension less than about 75 nanometers.

5. A semiconductor device, comprising:

a substrate;

a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area having at least one lateral dimension less than about 75 nanometers.

6. The semiconductor device in accordance with claim 5, further comprising:

a second semiconducting layer including a dopant of said second polarity formed over said base epitaxial semiconducting layer; and

a second junction formed between said epitaxial semiconducting base layer and said second semiconducting layer having a length and a width, and said second junction having an area having at least one lateral dimension less than about 75 nanometers.

7. The semiconductor device in accordance with claim 6, wherein said first semiconducting layer further comprises a first epitaxial semiconducting layer, wherein said base epitaxial semiconducting layer, said first epitaxial semiconducting layer, and said second semiconducting layer form a vertical bipolar transistor.

8. The semiconductor device in accordance with claim 6, further comprising an electrically conductive layer forming an ohmic contact to a portion of said base epitaxial semiconducting layer, and said electrically conductive layer forming a Schottky barrier to a portion of either said first or said second semiconducting layers, whereby a Schottky diode clamped bipolar junction transistor is formed.

9. An integrated circuit comprising:

at least one semiconductor device of claim 6; and

a transistor control circuit coupled to said at least one semiconductor device.

10. The semiconductor device in accordance with claim 5, wherein said substrate further comprises a semiconductor substrate having a dopant of said second polarity, wherein said semiconductor substrate forms said first semiconductor layer.

11. The semiconductor device in accordance with claim 5, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

12. The semiconducting device in accordance with claim 11, further comprising a plurality of second semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

13. The semiconducting device in accordance with claim 11, wherein said substrate further comprises a dielectric layer disposed between said substrate and said epitaxial semiconducting base lines.

14. The semiconducting device in accordance with claim 11, wherein said epitaxial semiconducting base lines and said first and second semiconducting lines form a hexagonal array.

15. The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines are substantially mutually orthogonal to said plurality of epitaxial semiconducting base lines.

16. The semiconductor device in accordance with claim 11, wherein said predetermined angle is between about 20 degrees and about 90 degrees.

17. The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines and said plurality of epitaxial semiconducting base lines form a diode array having an areal density in the range from about 0.2 Tera diodes/cm^2 to about 10.0 Tera diodes/cm^2.

18. The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines and said plurality of epitaxial semiconducting base lines form a bipolar junction transistor array having an areal density in the range from about 0.2 Tera transistors/cm^2 to about 10.0 Tera transistors/cm^2.

19. The semiconductor device in accordance with claim 5, wherein said first junction further comprises an area of less than about 15,000 square nanometers.

20. The semiconductor device in accordance with claim 5, wherein said substrate further comprises a dielectric layer disposed between said substrate and said base epitaxial semiconducting layer.

21. The semiconductor device in accordance with claim 5, wherein said base epitaxial semiconducting layer further comprises a thickness in the range from about 1.0 nanometer to about 1,000 nanometers.

22. An electronic device, comprising:

an integrated circuit including at least one semiconductor device of claim 5.

23. A computer system, comprising:

a microprocessor;

an electronic device including at least one semiconductor device of claim 5 coupled to said microprocessor; and

memory coupled to said microprocessor, said microprocessor operable of executing instructions from said memory to transfer data between said memory and the electronic device

24. The computer system in accordance with claim 23, wherein said electronic device is a storage device.

25. The computer system in accordance with claim 23, wherein said electronic device is a display device.

26. The computer system in accordance with claim 23, wherein said memory further comprises an integrated circuit including at least one semiconductor device having:

a substrate;

an base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area having at least one lateral dimension less than about 75 nanometers.

27. The computer system in accordance with claim 26, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

28. The computer system in accordance with claim 23, wherein said microprocessor further comprises an integrated circuit including at least one semiconductor device having:

a substrate;

an base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area having at least one lateral dimension less than about 75 nanometers.

29. The computer system in accordance with claim 28, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

30. A bipolar junction transistor comprising:

a semiconductor substrate having a substantially planar surface including a dielectric layer formed on or within said substrate;

a first epitaxial semiconducting structure including a dopant of a first polarity disposed on said dielectric layer, said first epitaxial semiconducting structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers;

a second epitaxial semiconducting structure including a dopant of a second polarity formed on said first epitaxial semiconductor structure, said second epitaxial semiconducting structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers;

a third epitaxial semiconducting structure including a dopant of said first polarity formed on said second epitaxial semiconductor sturcture, said third epitaxial structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers; and

an electrically conductive layer forming an ohmic contact to a portion of said second epitaxial semiconducting structure, and said electrically conductive layer forming a Schottky barrier to a portion of either said first or said third epitaxial semiconducting structures, whereby a Schottky diode clamped bipolar junction transistor is formed.

31. A bipolar junction transistor, comprising:

a semiconductor substrate having a substantially planar surface including a dielectric layer formed on said substrate

an epitaxial semiconducting structure formed on said dielectric layer, said epitaxial structure having an area having at least one lateral dimension less than about 75 nanometers, and forming a base region of the bipolar junction transistor;

a first polycrystalline semiconducting structure, formed on at least a portion of said epitaxial structure, said first polycrystalline structure having an area having at least one lateral dimension less than about 75 nanometers, and forming an emitter region of the bipolar junction transistor; and

a second polycrystalline semiconducting structure formed on at least a portion of said epitaxial structure, said second polycrystalline structure having an area having at least one lateral dimension less than about 75 nanometers, and forming a collector region of the bipolar junction transistor.

32. A diode array, comprising:

a silicon semiconductor wafer;

an insulating layer disposed over said silicon wafer;

a plurality of epitaxial semiconducting structures having an area having at least one lateral dimension less than about 75 nanometers, said plurality of epitaxial structures disposed over said insulating layer; and

a plurality of polycrystalline semiconducting structures having an area having at least one lateral dimension less than about 75 nanometers, said plurality of polycrystalline structures in contact with said plurality of epitaxial structures, forming an array of semiconducting junctions.

33. A semiconductor device comprising:

a substrate;

an epitaxial semiconducting structure formed on said substrate;

a polycrystalline semiconducting structure; and

means for forming a first semiconducting junction between said epitaxial semiconductor structure and said polycrystalline semiconducting structure, said semiconducting junction having an area having at least one lateral dimension less than about 75 nanometers.

34. The semiconductor device in accordance with claim 33, further comprising: means for forming a second semiconducting junction between said epitaxial semiconductor layer and said substrate, said second semiconducting junction having an area having at least one lateral dimension less than about 75 nanometers.

35. A method for forming nanoscale semiconductor junctions comprising:

creating an epitaxial semiconducting layer including a dopant of a first polarity formed on a complementary doped semiconductor substrate;

creating an imprint layer on said epitaxial semiconducting layer;

urging a nanoimprinter toward said imprint layer;

removing selective portions of said epitaxial semiconducting layer

forming an epitaxial semiconducting structure having an area having at least one lateral dimension less than about 75 nanometers;

creating a dielectric layer over said epitaxial semiconducting structure;

co-planarizing said dielectric layer to substantially the same thickness as said epitaxial semiconducting structure;

creating a polycrystalline semiconducting layer including a dopant of a second polarity over said epitaxial semiconducting layer and said dielectric layer;

removing selective portions of said polycrystalline semiconducting layer; and

forming a polycrystalline semiconducting structure having an area having at least one lateral dimension less than about 75 nanometers by selectively removing portions of said polycrystalline semiconducting layer.

36. A bipolar junction transistor created by the method of claim 35.

37. A method for forming nanoscale semiconductor junctions comprising:

creating an imprint layer on an epitaxial semiconducting layer;

urging a nanoimprinter toward said imprint layer;

removing selective portions of said epitaxial semiconducting layer;

forming an epitaxial semiconducting structure having an area having at least one lateral dimension less than about 75 nanometers; and

forming a first semiconducting junction having an area having at least one lateral dimension less than about 75 nanometers.

38. The method in accordance with claim 37, further comprising creating said epitaxial semiconducting layer on a complementary doped semiconductor substrate, wherein said epitaxial semiconducting layer includes a dopant of a first polarity.

39. The method in accordance with claim 38, further comprising creating a dielectric layer between said substrate and said epitaxial semiconducting layer.

40. A bipolar junction transistor created by the method of claim 37.

41. The method in accordance with claim 37, further comprising:

creating a first planarizing dielectric layer over said epitaxial semiconducting structure;

co-planarizing said first planarizing dielectric layer to substantially the same thickness as said epitaxial semiconductor structure;

creating a second semiconducting layer including a dopant of a second polarity over said epitaxial semiconducting layer and said first planarizing dielectric layer;

creating a second imprint layer on said second semiconducting layer;

urging a nanoimprinter toward said second imprint layer;

removing selective portions of said second semiconducting layer; and

forming a second semiconducting structure having an area having at least one lateral dimension less than about 75 nanometers.

42. The method in accordance with claim 41, further comprising forming a second semiconducting junction having an area having at least one lateral dimension less than about 75 nanometers.

43. A bipolar junction transistor created by the method of claim 41.

44. The method in accordance with claim 41, wherein creating a second semiconducting layer further comprises creating a doped polysilicon layer.

45. The method in accordance with claim 41, wherein forming said epitaxial semiconductor structure further comprises forming a plurality of epitaxial semiconducting lines substantially parallel to each other, and forming said second semiconducting structure further comprises forming a plurality of second semiconducting lines substantially parallel to each other, and at a predetermined angle to said plurality of epitaxial semiconducting lines.

46. The method in accordance with claim 37, further comprises removing a recessed portion.

47. The method in accordance with claim 37, further comprises creating an etch mask over portions of said imprinting layer and portions of said epitaxial semiconducting layer.

48. The method in accordance with claim 47, further comprising removing said etch mask.

49. The method in accordance with claim 47, wherein creating said etch mask further comprises:

creating a diffusion barrier over portions of said imprinting layer and portions of said epitaxial semiconducting layer; and

creating and electrically conductive layer over said diffusion barrier.

50. The method in accordance with claim 47, further comprising forming an electrical contact to said epitaxial semiconducting layer utilizing said diffusion barrier and said electrically conductive layer.

51. The method in accordance with claim 37, further comprising removing said implant layer.

52. The method in accordance with claim 51, further comprising plasma cleaning an exposed surface of said epitaxial semiconducting layer.

53. The method in accordance with claim 37, wherein said urging a nonoimprinter further comprises heating said implant layer.

54. The method in accordance with claim 37, further comprising etching said epitaxial semiconducting layer.

55. The method in accordance with claim 37, wherein creating said imprinting layer further comprises depositing said imprinting layer utilizing inkjet deposition.

56. A method for forming nanoscale junctions comprising:

creating a doped epitaxial silicon layer, which has a thickness less than about 75 nanometers, on a doped silicon wafer;

urging a nanoimprinter toward an imprint layer

removing selective portions of said doped epitaxial silicon layer;

forming a semiconductor junction between said doped silicon wafer and said epitaxial silicon layer having an area having at least one lateral dimension less than about 75 nanometers;

forming a planarizing dielectric layer over said doped epitaxial silicon structure;

co-planarizing said planarizing dielectric layer to substantially the same thickness as said doped epitaxial silicon structure;

creating a second semiconducting layer over said epitaxial silicon structure and said planarizing dielectric layer, said semiconducting layer having a dopant opposite in polarity to said epitaxial silicon layer;

urging a nanoimprinter toward a second imprint layer;

removing selective portions of said second semiconducting layer; and

forming a second semiconductor junction between said doped epitaxial layer and said second semiconducting layer having an area having at least one lateral dimension less than about 75 nanometers.